



Certification Process: Server and Storage

Tokyo, 2014

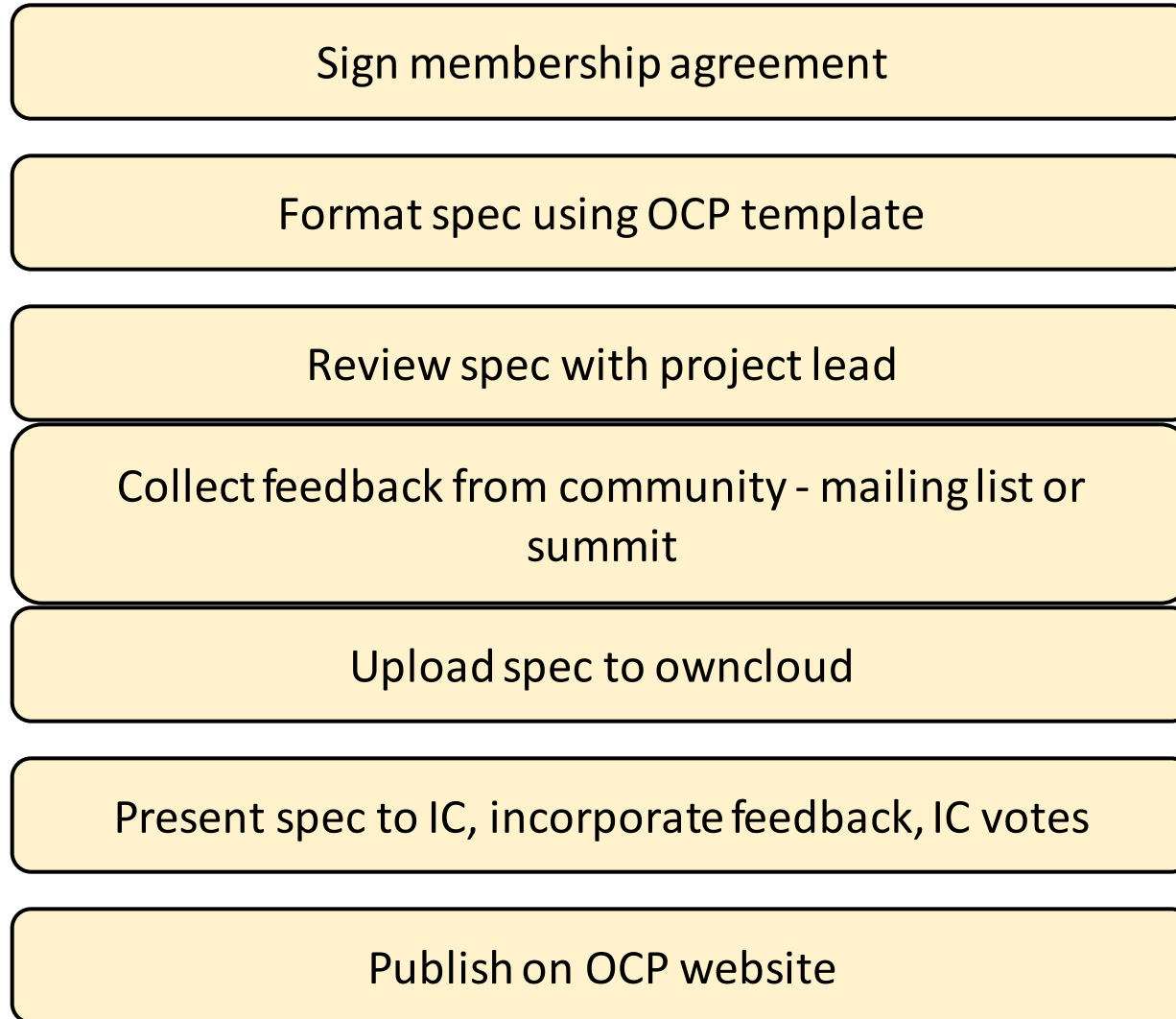


Certifying an OCP Machine

1. An specification needs to be approved by Incubation Committee (IC)
2. Certification/C&I project develops certification spec
3. Testing tool development on target platforms
4. Certification specification becomes official
5. Vendor submits for certification
6. Certified status granted by OCP Foundation
7. Results are published

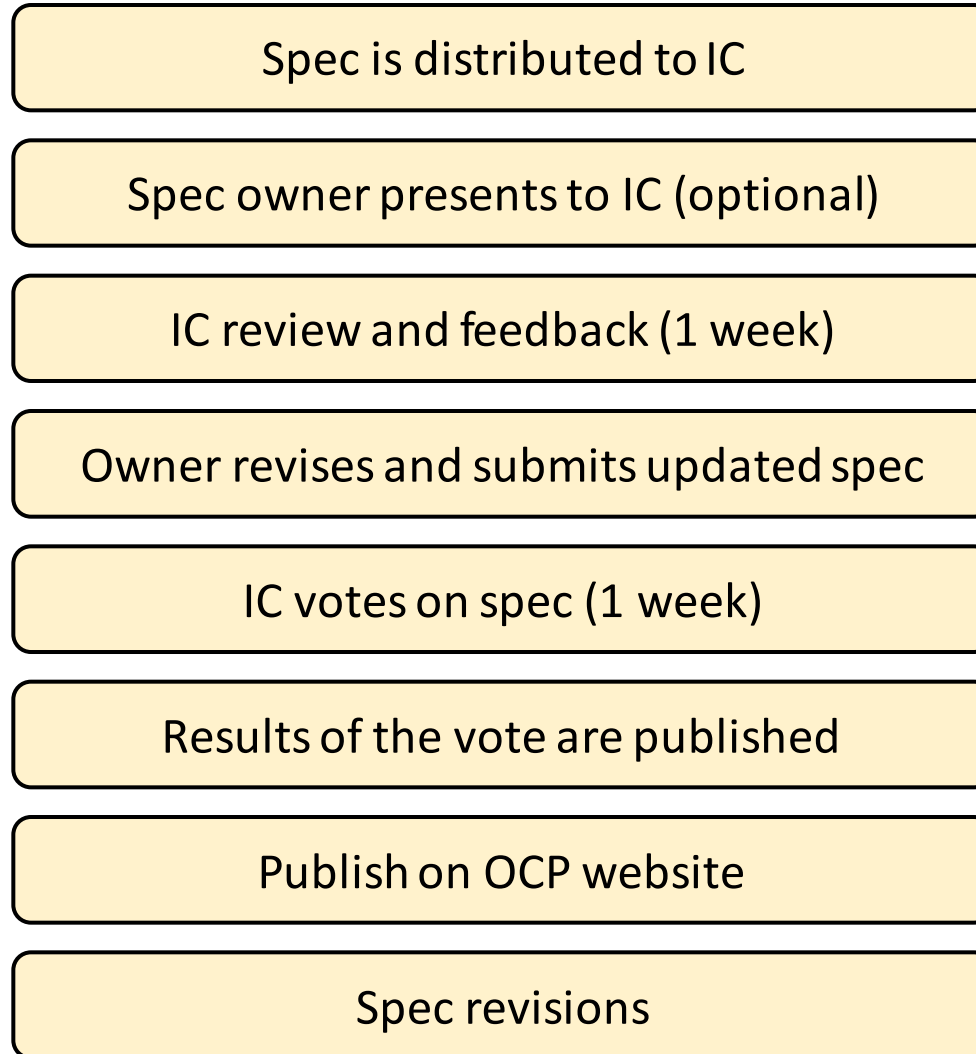
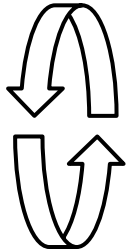


OCP Project Submission





IC voting process



IC/Project Partnerships

Chair: Andreas Bechtolsheim - Arista Networks

Vice-Chair: Amir Michael - Coolan/OCP Co-
Founder

Bob Ogrey - AMD

Server - Mark Shaw,

Chilung Wang - ITRI

Hardware Management - Rajeev
Agrawala / Badriddine Khessib

Matt Corddry - Facebook

Open Rack - Steve Mills / Brian
Obernesser

Aaron Sullivan - Rackspace

Certification - YF Juan

Conor Malone - Hyve Solutions

Storage - Asghar Riahi

Bill Carter - Intel

Data Center - Jason S Schafer

Kushagra Vaid - Microsoft

Networking - Omar Baldonado /
Carlos Cardenas



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Certifying an OCP Server

ITRI OCP Certification Testing Center Operations:

- Workflow processes
- Results examples
- Lessons learnt



- Workflow processes
- Results examples
- Lessons learnt

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Submission Request

OCP Certification Request (Form: OCP-CI-0004)

Contact Information

Company Name			
Address			
Business contact			
Name		email address	
mobile		office	
Technical contact			
Name		email address	
mobile		office	
Logistic/administrative contact			
Name		email address	
mobile		office	

Submission info (Please select certification category)	
<input type="checkbox"/>	Server
<input type="checkbox"/>	Storage

SUT Spec

140CP-CI-0005: OCP Certification SUT Specification

(工程規格表單)

Specification		Inventory Information		Volume	Check?
Item	Description	Item	Description		
Model Name	<i>for example:</i> Windmill-EP FAB7	SUT1	GUID (unique) <i>for example:</i> 00020003-0004-0005-0600-000700	SUT	Sample Sizes 3
Physical Dimension	<i>for example:</i> Length: --; Width: --;		MAC address <i>for example:</i> 1G LAN MAC: xx:xx:xx:xx:xx:xx, BMC MAC: xx:xx:xx:xx:xx:xx; 10G LAN MAC: xx:xx:xx:xx:xx:xx, BMC MAC: xx:xx:xx:xx:xx:xx;		
BIOS version	<i>for example:</i> EP_ID07	SUT2	GUID (unique) <i>for example:</i> 00020003-0004-0005-0600-000700	N/A	
ME version	<i>for example:</i> 2.17		MAC address <i>for example:</i> 1G LAN MAC: xx:xx:xx:xx:xx:xx,		
CPU	<i>for example:</i> Intel(R) Xeon(R) CPU E5-2660, 2.20GHz, L3 20MB				

Information prepared and material provided to Lab:



Email Notification

From: ITRI OCP Lab
To:
Cc: CCMA-ZGP31 (OCP Team)
Subject: 設備收受確認

您好，
工服單No.66-OCP-2013-005-A
本實驗室已於2013年12月27日17時收取，
比對確認貴公司提供之設備清單型號及數量無誤，
特此告知，將如期展開測試，如有任何問題敬請來信洽詢。
謝謝您！
OCP Lab ITRI

Jira Tracking

OCP C&I / OCP-76
66-OCP-2013-005-A Wiwynn Winterfell Formal Submission

[Edit](#)
[Assign](#)
[Assign To Me](#)
[Comment](#)
[More Actions](#)
[Resolve Issue](#)
[Workflow](#)

35.	✓	JIRA35-(66-OCP-2013-005-A)-更新66-OCP-2013-005-A-summary.xlsx	📄	👤 Closed	朱逸勤	⬆️	⚙️
36.	✓	JIRA36-(66-OCP-2013-005-A)-整合報表產出 OCP C&I Test Report File Name Rule: 66-OCP-2013-005-A.docx	📄	👤 Closed	吳書瑋	⬆️	⚙️
37.	✓	JIRA37-(66-OCP-2013-005-A)-Progress Notification Email Stage 3: 完成所有測試	📄	👤 Closed	吳書瑋	⬆️	⚙️
38.	✓	JIRA38-(66-OCP-2013-005-A)-實驗室管理者檢視報告	📄	👤 Closed	李珊	⬆️	⚙️
39.	✓	JIRA39-(66-OCP-2013-005-A)-組長檢視報告	📄	👤 Closed	王啓龍	⬆️	⚙️



- Workflow processes
- Results examples (Wiwynn submission)
- Lessons learnt



P. 7: CPU

SUT1 Test Result

Test Case No.	Description	Result
TC-001-0001-001	<ol style="list-style-type: none"> Gathering CPU information by using lshw command. Output CPU model and L1, L2, L3 cache size. Criteria: CPU model should belong to Intel® Xeon® processor E5-2600 product family and L3 Cache should be larger than 20MB 	<p>Intel(R) Xeon(R) CPU E5-2660 v2 @ 2.20GHz CPU Internal L1 640 KB CPU Internal L2 2 MB CPU Internal L3 25 MB</p> <p>Intel(R) Xeon(R) CPU E5-2660 v2 @ 2.20GHz CPU Internal L1 640 KB CPU Internal L2 2 MB CPU Internal L3 25 MB</p>
TC-001-0001-002	<ol style="list-style-type: none"> Gathering CPU information by using lscpu command. Output the total number of CPU, the number of Thread per core, the number of Core per Socket, and the number of Socket. Criteria: It should be 8-12 cores per CPU and 2 Threads per core. 	<p>CPU(s): 40</p> <p>Thread(s) per core: 2</p> <p>Core(s) per socket: 10</p> <p>Socket(s): 2</p>

P. 9-10: Temperature

TC-001-0006-001	<ol style="list-style-type: none"> Retrieving CPU, DIMM, chipset, inlet, outlet temperature via DCMI in-band access using dcmi tool. The motherboard has five thermal sensors: Two for CPU0 and CPU1 	<p>Outlet Temp: 25 degrees C</p> <p>Inlet Temp: 20 degrees C</p> <p>PCH Temp: 48 degrees C</p> <p>P0 DIMM Temp: 29 degrees C</p> <p>P1 DIMM Temp: 30 degrees C</p>
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Open Compute Project Compliance & Interoperability Test Report

	<p>temperatures, Two for CPU0 DIMM group and CPU1 DIMM group temperatures, one for PCH temperature, one for Inlet temperature, one for outlet temperature.</p> <ol style="list-style-type: none"> Criteria: These five temperatures should be able to be retrieved via DCMI in-band access. 	<p>CPU0 Temp: 31 degrees C</p> <p>CPU1 Temp: 32 degrees C</p>
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P. 12: Power Reset

<p>TC-002-0006-002</p>	<ol style="list-style-type: none"> 1. Power reset the SUT using dcmitool through out-of-band access 20 times. 2. Criteria: The SUT should be successfully powered reset 20 times by dcmitool out-of-band access. 	<p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p> <p>10.2.103.5 Chassis Power Control: Reset</p>
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P. 13-14: ID Check

TC-002-0010-001	<ol style="list-style-type: none"> Retrieving inventory information via dcmi tool. Asset Tag can be set. Retrieving inventory information which contains Device ID, System GUI, 	<p>Asset Tag: 66-OCP-2013-005-A-SUT1</p> <p>System GUID: c6d65b07-535e-e311-7ba7-b2d71e3a3201</p> <p>Get Management Controller Identifier String:</p> <p>DCMI0002C9B29A6C</p> <p>Device ID: 80</p>
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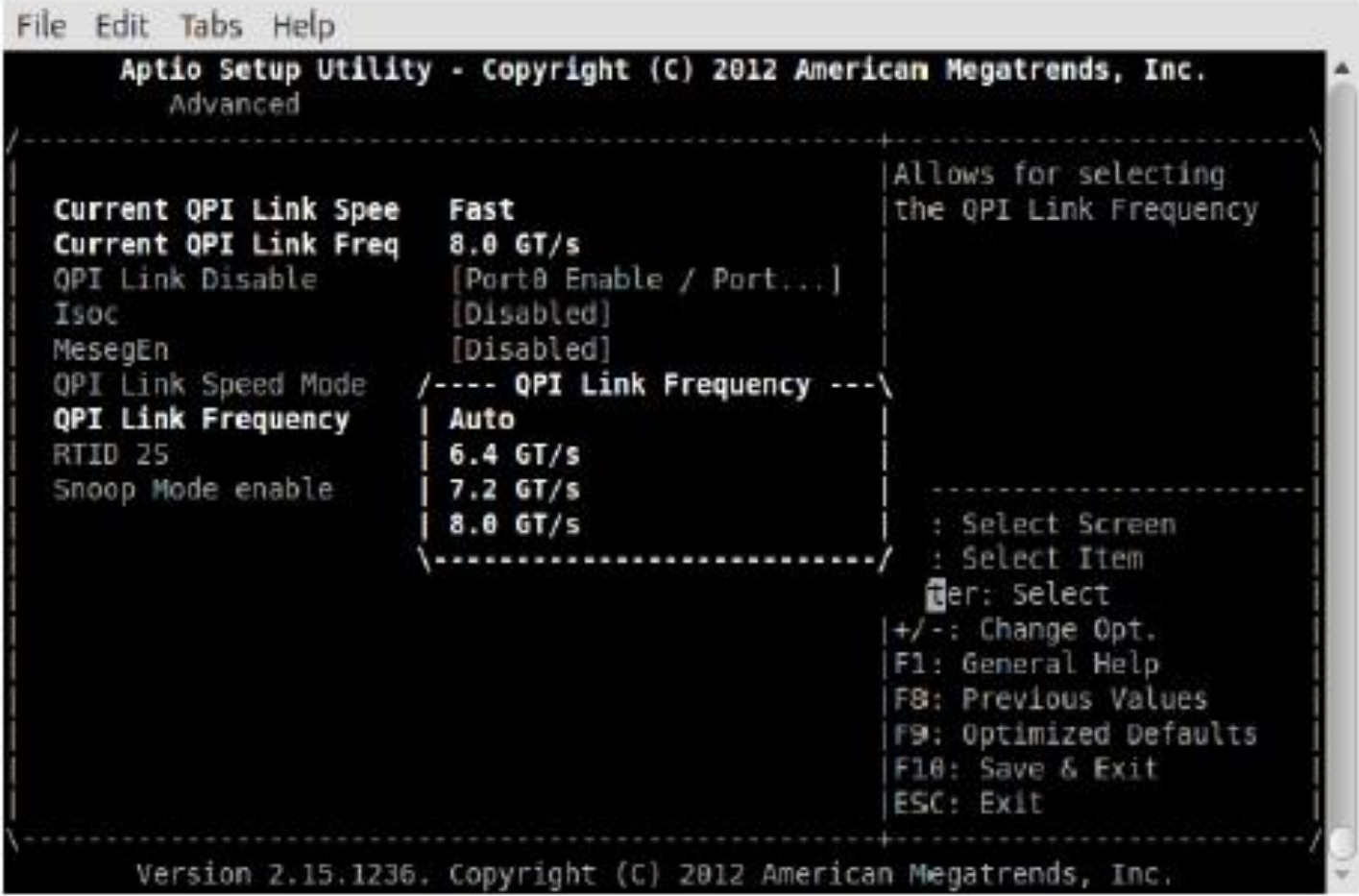
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Open Compute Project Compliance & Interoperability Test Report

	<p>Firmware/Software Information, Management Controller ID.</p> <ol style="list-style-type: none"> Criteria: All information mentioned above should not be null. 	<p>Manufacturer Name: Intel Corporation</p> <p>Firmware Revision: 2.17</p>
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P. 40: BIOS

Figure Name	QPI speed
Figure	 <pre> File Edit Tabs Help Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc. Advanced ----- Current QPI Link Spee Fast Current QPI Link Freq 8.0 GT/s QPI Link Disable [Port0 Enable / Port...] Isoc [Disabled] MesegEn [Disabled] QPI Link Speed Mode /---- QPI Link Frequency ----\ QPI Link Frequency Auto RTID 25 6.4 GT/s Snoop Mode enable 7.2 GT/s 8.0 GT/s \-----/ : Select Screen : Select Item Enter: Select +/-: Change Opt. F1: General Help F8: Previous Values F9: Optimized Defaults F10: Save & Exit ESC: Exit Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc. </pre>



P. 42: Power Restore





Report Statistics

- Page Count: 81
- Page 1: Cover Page
- Page 2: Certification Results Source
- Page 3-6: Test/Sample Description
- Page 7-39: Test Results (Text-based)
- Page 40-81: Appendix (screen shots)



Agenda

- Workflow processes
- Results examples
- Lessons learnt



Information Collection

- SUT Spec: configurations for all systems **MUST** be identical
 - For example, if each machine uses different DIMM, it will be sent back
- PXE Boot: must have MAC address



Vendor Settings

- Sensor ID naming conventions
 - Each vendor is different, ITRI had to ask/confirm individually
 - Current process is liable to human errors
- BIOS default settings
 - Each vendor is different, ITRI had to ask/confirm individually
 - Current process is liable to human errors



Logs Issues

```
ccma@winterfell:~$ dcmi tool -H 10.2.103.5 -U USERID -P PASSWORD sel list
1 | 12/12/2013 | 05:35:23 | OEM 10x5f | | Asserted
2 | 02/07/2106 | 06:28:15 | OEM 10x70 | | Asserted
3 | 01/01/2011 | 00:00:03 | System Firmware Error 10x2b | Unknown Error | Asserted
4 | 01/01/2011 | 00:01:10 | System Firmware Error 10x2b | Unknown Error | Asserted
5 | 01/01/2011 | 00:02:22 | Battery 10x45 | Low | Asserted
```

- “System Firmware Error”
 - Message lacks granularity
 - ITRI had to call and confirm this is the expected behavior (when battery is unplugged)
 - Suggest that vendor provide more granular information



Services

Submit

FAQ

Participate

About

Contact



Open Computer Project Certification Testing Center

- > Who We Are
- > Requirements
- > Methodologies
- > Tested Systems

Tested Systems

Company	Category	Model Name	Common Name	Date Tested	Specifications	Details
Quanta Computer Inc.	Server	F03C	Winterfell	24-Jan-14	Intel v. 2.0 Spec	
Wiwynn Corp.	Server	Winterfell	Winterfell	7-Jan-14	Intel v. 2.0 Spec	

URL: [www. OCP Certification Center .org](http://www.OCP Certification Center .org)



Certify Knox/Cold Storage

1. Spec: Knox/OpenVault v0.8+
2. Partners: Seagate, UTSA, ITRI, Canonical
3. Certification spec: v0.13
4. Certification Package: please join us
5. Target platform: TBD



工業技術研究院
Industrial Technology
Research Institute



Q&A

Thank You

Y.F. Juan / 阮耀飛

Deputy Director

Global Strategy & Business Development

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